

April 23, 2002 (now U.S. Patent No. 6,531,915), which is a continuation of U.S. Patent Application No. 09/712,413 (now U.S. Patent No. 6,396,335 B1), which claims the benefit of U.S. Provisional Application No. 60/164,988 filed November 11, 1999, all of which are incorporated herein by reference in their entirety.

In the Claims:

Please cancel claims 1-18 without prejudice or disclaimer, and add claims 19-23.

1. (canceled)
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18. canceled)

19. (new) A current mirror circuit, comprising:

a reference current side having a first transistor and a second transistor, a source of said first transistor coupled to a drain of said second transistor; and

a load current side having a third transistor, a gate of said third transistor connected to a gate of said second transistor, a drain of said third transistor connected to a load circuit;

wherein a drain-to-source voltage drop across said second transistor matches a drain-to-source voltage drop across said third transistor.

20. (new) The current mirror circuit of claim 19, wherein a reference current in said reference current side tracks changes of a load current in said load current side.

21. (new) The current mirror of claim 20, wherein said reference current is scaled relative to said load current.

22. (new) A current mirror circuit, comprising:

a reference current side having a first transistor and a second transistor, a source of said first transistor coupled to a drain of said second transistor; and

a load current side having a third transistor, a gate of said third transistor connected to a gate of said second transistor, a drain of said third transistor connected to a load circuit;

wherein said load current side supplies a load current to said load circuit, and said reference current side generates a reference current that is proportional to said load current so that said reference current tracks changes in said load current.

23. (new) A method for maintaining a current ratio in a current mirror circuit, the current mirror having a reference current side with a first transistor coupled to a second transistor, and a load current side having a third transistor with a gate connected to a gate of the second transistor, comprising:

generating a reference current in the reference current side;

generating a load current in the load current side that is proportional to the reference current generated in the reference current side; and

causing a drain-to-source voltage drop across said second transistor to match a drain-to-source voltage drop across said third transistor so that said reference current tracks changes in said load current.